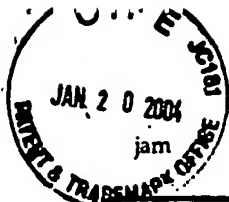




Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO:** Assistant Commissioner for Patents, Washington, DC 20231.



Substitute for form 1449A/PTO			Complete if Known		
			Application / C n. N .	10/082,630 / 4447	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Filing Dat	February 22, 2002	
			First Named Invent r	Robert Yin	
			Art Unit	2819	
			Examiner Name	Unknown	
Sheet	1	of	7	Attorney Docket Number	X-1070 US

U.S. PATENT DOCUMENTS						
Examiner Initials *	Cite No. *	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (If known)				
 		US-	4,758,985	07-19-88	Carter	
		US-	5,142,625	08-25-92	Nakai	
		US-	4,855,669	08-08-89	Mahoney	
		US-	34,363	08-31-93	Freeman	
		US-	5,072,418	12-10-91	Boutaud et al.	
		US-	5,274,570	12-28-93	Izumi et al.	
		US-	5,550,782	08-27-96	Cliff et al.	
		US-	5,347,181	09-13-94	Ashby et al.	
		US-	5,339,262	08-16-94	Rostoker et al.	
		US-	5,311,114	05-10-94	Sambamurthy et al.	
		US-	5,504,738	04-02-96	Sambamurthy et al.	
		US-	5,552,722	09-03-96	Kean	
		US-	6,467,009	10-15-02	Winegarden et al.	
		US-	5,914,616	06-22-99	Young et al.	
		US-	5,457,410	10-10-95	Ting	
		US-	5,740,404	04-14-98	Baji	
		US-	5,581,745	12-03-96	Muraoka	
		US-	5,742,179	04-21-98	Sasaki	
		US-	5,600,845	02-04-97	Gilson	
		US-	5,574,930	11-12-96	Halverson Jr., et al.	

RECEIVED
JAN 22 2004
Technology Center 210

RECEIVED
JAN 22 2004
TECHNOLOGY CENTER 210

RECEIVED

JAN 22 2004

Technology Center 210

RECEIVED
JAN 22 2004
TECHNOLOGY CENTER 2800

FOREIGN PATENT DOCUMENTS						
Examiner Initials *	Cite No. *	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code *	Number - Kind Code * (if known)			
		EP	0315275 A2	10-05-89	LSI Logic	
		WO	93 25968 A1	12-23-93	Furtek	
		EP	0 905 906 A2	03-31-99	Lucent	
		EP	1 235 351 A1	08-28-02	Matsushita Electric	

Examiner Signature		Date Considered	12/7/04
--------------------	--	-----------------	---------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

* Applicant's unique citation designation number (optional). * See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. * Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). * For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. * Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. * Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, P.O. Box 1450, Alexandria, Virginia, 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia, 22313-1450.



PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 7

Complete If Known

Application / Conf. N .	10/082,630 / 4447
Filing Dat	February 22, 2002
First Named Inventor	Robert Yin
Art Unit	2819
Examiner Name	Unknown
Attorney Docket Number	X-1070 US Technology Center 2100

OTHER - NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T *
df	/	SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
df	/	VASON P. SRINI, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
df	/	G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
df	/	JACOB DAVIDSON, "FPGA IMPLEMENTATION OF RECONFIGURABLE MICROPROCESSOR," IEEE, March 1993, pp. 3.2.1 - 3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
df	/	CHRISTIAN ISELI et al., "BEYOND SUPERSCALER USING FPGA's," IEEE, April 1993, pp. 486-490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
df	/	P.C. FRENCH et al., "A SELF-RECONFIGURING PROCESSOR," IEEE, July 1993, pp. 50-59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
df	/	Christian Iseli et al., "SPYDER: A RECONFIGURABLE VLIW PROCESSOR USING FPGA's," IEEE, July 1993, pp. 17-24, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
df	/	MICHAEL J. WIRTHLIN et al., "THE NANO PROCESSOR: A LOW RESOURCE RECONFIGURABLE PROCESSOR," IEEE, February 1994, pp. 23-30, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
df	/	WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
df	/	ANDRE DEHON, "DPGA-COUPLED MICROPROCESSORS: COMMODITY ICs FOR THE EARLY 21ST CENTURY," IEEE, February 1994, pp. 31 - 39, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
df	/	OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

Examiner
Signature

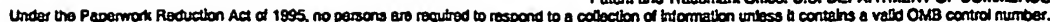
Date
Considered

12/7/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

* Applicant's unique citation designation number. * Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

**Complete if Known**

Applicati n / C nf. No.	10/082,630 / 4447
Filing Dat	February 22, 2002
First Named Inventor	Robert Yin
Art Unit	2819
Examiner Name	Unknown
Attorney Docket Number	X-1070 US

(use as many sheets as necessary)

Sheet	3	of	7
-------	---	----	---

U.S. PATENT DOCUMENTS					
Examiner Initials *	Cite No.¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
R ↓ R		US- 5,473,267	12-05-93	Stansfield	
		US- 5,742,180	04-21-98	DeHon et al.	
		US- 5,737,631	04-07-98	Trimberger	
		US- 5,748,979	05-05-98	Trimberger	
		US- 6,578,174	06-10-03	Zizzo	RECEIVED
		US- 6,026,481	02-15-00	New et al.	
		US- 5,705,938	01-06-98	Kean	JAN 22 2004
		US- 5,500,943	03-19-96	Ho et al.	
		US- 6,483,342	11-19-02	Britton et al.	Technology Center 2100
		US- 5,809,517	09-15-98	Shimura	
		US- 5,543,640	08-06-96	Sutherland et al.	
		US- 5,574,942	11-12-96	Colwell et al.	
		US- 6,604,228	08-05-03	Patel et al.	
		US- 5,933,023	08-03-99	Young	
		US- 10/043,769	01-09-02	Schulz	
		US- 6,389,558	05-14-02	Herrmann et al.	
		US- 5,732,250	03-24-98	Bates et al.	
		US- 5,889,788	03-30-99	Pressly et al.	
	US- 5,874,834	02-23-99	New		
	US- 5,835,405	11-10-98	Tsur et al.		

[illegible]

Date Considered

BURDEN HOUR STATEMENT: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, P.O. Box 1450, Alexandria, Virginia, 22313-1450. DO NOT SEND FEES. R
COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia, 22313-1450.



PTO/SB/08A (10-01)

Approved for use through 10/31/2002. OMB 0651-0031

Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 4 of 7

Complete If Known

Application / Cnt. N.	10/082,630 / 4447
Filing Date	February 22, 2002
First Named Inventor	Robert Yin
Art Unit	2819
Examiner Name	Unknown
Attorney Docket Number	X-1070 US

RECEIVED

JAN 22 2004

OTHER - NON PATENT LITERATURE DOCUMENTS

Technology Center 2100

Examiner Initials *	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issues number(s), publisher, city and/or country where published.	T *
BP	/	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
BP	/	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
BP	/	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-9 to 2-18; 2-187 to 2-199, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
BP	/	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-107 to 2-108, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
BP	/	CHRISTIAN ISELI et al., "AC++ COMPILER FOR FPGA CUSTOM EXECUTION UNITS SYNTHESIS," 1995, pp. 173-179, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
BP	/	INTERNATIONAL BUSINESS MACHINES, "POWERPC 405 EMBEDDED PROCESSOR CORE USER MANUAL," 1996, 5TH Ed., pp. 1-1 TO X-16, International Business Machines, 1580 Rout 52, Bldg. 504, Hopewell Junction, NY 12533-6531.	
BP	/	YAMIN LI et al., "AIZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
BP	/	RALPH D. WITTIG et al., "ONECHIP: AN FPGA PROCESSOR WITH RECONFIGURABLE LOGIC," April 17, 1996, pp 126-135, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
BP	/	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," January 27, 1999, Ch. 3, pp 3-1 TO 3-50, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
BP	/	WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
BP	/	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	

Examiner
SignatureDate
Considered

12/7/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.


* Applicant's unique citation designation number. * Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.



PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO			Complete if Known		
			Applicant / Cnf. No.	10/082,630 / 4447	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT			Filing Date	February 22, 2002	
			First Named Inventor	Robert Yin	
(use as many sheets as necessary)			Art Unit	2819	
			Examiner Name	Unknown	
Sheet	5	of	7	Attorney Docket Number	X-1070 US

U.S. PATENT DOCUMENTS						
Examiner Initials *	Cite No.¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)				
		US-	6,011,407	01-04-00	New	
		US-	6,172,990	01-09-01	Deb et al.	
		US-	10/001,871	11-19-01	Douglass et al.	
		US-	5,760,607	06-02-98	Leeds et al.	RECEIVED
		US-	5,892,961	04-06-99	Trimberger	
		US-	09/991,412	11-16-01	Herron et al.	JAN 22 2004
		US-	09/991,410	11-16-01	Herron et al.	
		US-	09/968,446	09-28-01	Douglass et al.	Technology Center 2100
		US-	6,178,541	01-23-01	Joly et al.	
		US-	2003/0062922	04-03-03	Douglass et al.	
		US-	2001/0049813	12-06-01	Chan et al.	
		US-	5,914,902	06-22-99	Lawrence et al.	
		US-	6,510,548	01-21-03	Squires	
		US-	6,154,051	11-28-00	Nguyen et al.	
		US-	6,181,163	01-30-01	Agrawal et al.	
		US-	6,356,987	03-12-02	Aulas	
		US-	6,301,696	10-09-01	Lien et al.	
		US-	6,211,697	04-03-01	Lien et al.	
		US-	6,163,166	12-19-00	Bielby et al.	
		US-	6,272,451	08-07-01	Mason et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials *	Cite No. 1	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code *	-Number* -Kind Code * (if known)			

Examiner Signature		Date Considered	12/7/04
-----------------------	--	--------------------	---------

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

* Applicant's unique citation designation number (optional). * See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. * Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). * For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. * Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. * Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, P. . Box 1450, Alexandria, Virginia, 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P. . Box 1450, Alexandria, Virginia, 22313-1450.



Approved for use through 10/31/2002. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Complete if Known

Application / Conf. N .	10/082,630 / 4447
Filing Date	February 22, 2002
First Named Inventor	Robert Yin
Art Unit	2819
Examiner Name	Unknown
Attorney Docket Number	X-1070 US

Sheet 6 of 7

Examiner Initials *	Cite No*	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ^a
cy		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch 3, pp 3-7 TO 3-17; 3-76 TO 3-87, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
sp	-	INTERNATIONAL BUSINESS MACHINES, "PROCESSOR LOCAL BUS" Architecture Specifications, 32-Bit Implementation, April 2000, First Edition, V2.9, pp. 1-76, IBM Corporation, Department H83A, P.O. Box 12195, Research Triangle Park, NC 27709	
eg	/	XILINX, INC., "VIRTEX II PLATFORM FPGA HANDBOOK, December 6, 2000, v1.1, pp 33-75, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		RECEIVED	
		JAN 22 2004	
		Technology Center 2100	
		RECEIVED	
		JAN 22 2004	
		TECHNOLOGY CENTER 2800	

Technology Center 2100

RECEIVED
JAN 22 1994
TECHNOLOGY CENTER 28000

12/7/04

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO:** Assistant Commissioner for Patents, Washington, DC 20231.



Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Applicati n / C nf. No.	10/082,630 / 4447
Filing Date	February 22, 2002
First Nam d Inventor	Robert Yin
Art Unit	2819
Examiner Name	Unknown
Attorney Docket Number	X-1070 US

Technology Center 2100

12/7/09

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, P.O. Box 1450, Alexandria, Virginia, 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia, 22313-1450.**